Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **COLLECTOR Q1**
2. **BASE Q1**
3. **EMITTERS Q1 & Q2**
4. **BASE Q2**
5. **COLLECTOR Q2**
6. **BASE Q3**
7. **EMMITTER Q3**
8. **COLLECTOR Q3**
9. **BASE Q4**
10. **EMITTER Q4**
11. **COLLECTOR Q4**
12. **BASE Q5**
13. **EMITTER Q5 & SUBSTRATE**
14. **COLLECTOR Q5**

**.041”**

**.041”**

**1 14**

**2**

**3**

**4**

**5**

**6 7 8 9**

**13**

**12**

**11**

**10**

**\*APPLICATION NOTE:**

**SUBSTRATE MUST BE CONNECTED TO THE MOST NEGATIVE POINT IN THE EXTERNAL CIRCUIT TO MAINTAIN ISOLATION BETWEEN TRANSISTORS AND TO PROVIDE FOR NORMAL TRANSISTOR ACTION.**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: SEE NOTE\***

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .041” X .041” DATE: 7/7/22**

**MFG: SILICON SUPPLIES THICKNESS .016” P/N: LM3045**

**DG 10.1.2**

#### Rev B, 7/1